This feature is disclosed, for example, in original claim 5. Claims 5 and 6 have been amended to more clearly recite that "an oxide" in line 1 is the first oxide. Claim 9 has been amended to clarify that each step of in-situ steam generation oxidation is carried out at the recited temperature range. Claim 15 has been amended to correspond to claims 5 and 6. Claim 17 has been amended to correct its dependency to claim 14. Claims 20, 21 and 22 (Applicants' original numbering) have been renumbered to 19, 20 and 21, which is the only amendment to these claims.

The specification has been amended as discussed below to address the Examiner's points.

The drawings have been corrected as discussed below to address the Examiner's points.

Applicants respectfully request reconsideration of the application based on the foregoing amendments and the following remarks. Applicants respectfully submit that all of the claims 1-21 are now in condition for allowance.

Rejections Under 35 U.S.C. §103(a)

Claims 1, 5-9, 12, 13 and 17 stand rejected under 102(b) as anticipated (*sic*) by US 5,953,254, Pourkeramati, in view of Van Zant, Microchip Fabrication. Applicants can only assume that the Examiner intended to reject these claims as obvious, since as a matter of law the claims cannot be anticipated by a combination of references. Applicants proceed accordingly herein. In addition, claims 10 and 11 stand rejected as obvious over Pourkeramati in view of Van Zant and further in view of US 6,271,054, Ballantine et al. Since the latter rejection is based on the same two references, the latter rejection is discussed below together with the first rejection. Applicants respectfully traverse these rejections on the following grounds.

Claims 1, 14 and 18 have been amended to recite that both oxide layers are formed by in-situ steam generation (ISSG) oxidation of the underlying surface, silicon in the case of the first oxide (or tunnel oxide in claim 14 or bottom oxide in claim 18), and silicon nitride in the case of the top oxide. Since there is neither disclosure nor suggestion to apply ISSG oxidation both to the underlying silicon surface and to the silicon nitride surface in either of the cited references, Applicants respectfully submit that the presently pending claims patentably distinguish over the

asserted combination of cited references. Furthermore, with respect to claims 3 and 14-17, there is no suggestion in either reference to apply such methods to a two-bit EEPROM, such as the MIRRORBIT™ discussed in the specification. Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejections of Applicants' claims over these references.

Since the amendment of generic claim 1 is considered to render this claim allowable, Applicants request the Examiner to remove the restriction of claims 2-4, 14 and 18 and the claims dependent thereon, and to indicate the allowability of all of the pending claims. Thus, as noted above, Applicants respectfully submit that all of claims 1-21 are now in condition for allowance.

Rejection under 35 U.S.C. §112, Second Paragraph

Claim 5 stands rejected under Section 112, second paragraph as indefinite. Claim 5 has been amended. Applicants respectfully submit that amended claim 5 is free of any indefiniteness. Reconsideration and withdrawal of this rejection is respectfully requested.

Objection to Specification and Claims

The specification has been objected to for two minor informalities. These informalities have been corrected in the foregoing amendments of the specification. It is noted that, in addition to the amendment of the paragraph at page 7 to replace "34" with "34a, 34b", the term "charge" has been made plural, and the term "it" has been replaced with "each", to maintain proper grammar in the amended sentences. The misnumbered claims 20-22 have been renumbered herein as 19-21. Claims 5 and 6 have been amended to replace "an oxide" with "a first oxide" as requested by the Examiner.

Objection to Drawings

The Examiner pointed out that the stored charges 34a, 34b shown in Fig. 1 were erroneously shown in layer 28 instead of layer 30. In addition, reference numerals 10 and 40 have been applied to the general structures shown in Figs. 1 and 2 respectively, and reference

numeral 36 has been added to show the silicon surface in Fig. 3. Support for these numerals is in the specification, for example, at page 5, line 22, page 6, line 1, and page 8, line 26, respectively. Appropriately corrected drawing sheets are submitted herewith, both marked in red to indicate the changes, and as formal drawings.

Election/Restriction

As noted above, generic claim 1 is considered allowable. Accordingly, Applicants request the Examiner to put the claims 2-4, 14-16 and 18-21 back into the case.

Conclusion

For all the foregoing reasons, Applicants respectfully submit that the present application is in condition for allowance, and respectfully request notice to such effect.

If the Examiner considers that a telephone interview would be helpful to facilitate favorable prosecution of this application, the Examiner is invited to telephone the undersigned.

It is believed no fee is required for this filing. However, if a fee is required, please charge the fee to Deposit Account No. 18-0988, Order No. AF01120.

Respectfully submitted,
RENNER, OTTO, BOISSELLE & SKLAR, LLP

DATE: October 10, 2002

Thomas W. Adams, Reg. No. 35,047

The Keith Building
1621 Euclid Avenue
Nineteenth Floor
Cleveland, Ohio 44115
Ph: (216) 621-1113
Fax: (216)621-6165
B:\132\Adams-Tom\Client Files\AMD\PAF1120\amdAF1120.ROA1.wpd

APPENDIX

The amended specification as shown above has been amended as follows:

The paragraph at page 6, lines 12-19:

The following description of the process of the present invention is described in the context of an ONO structure suitable for use in a two-bit EEPROM device, such as the MIRRORBIT™ device. It is to be understood that, while the present invention is discussed herein in that context, that this is merely exemplary and is not intended to limit the scope of the present invention. The ONO structure fabricated by the presently disclosed method is applicable to any semiconductor device in which an ONO structure may be included, and is particularly applicable also to the floating gate FLASH device described above with reference to Fig. 2.

The paragraph at page 7, lines 3-11:

Those skilled in the art will recognize that for proper functioning of a two-bit EEPROM device, the electrical [charge 34] charges 34a, 34b should remain isolated in the regions of the silicon nitride layer 30 to which [it] each is initially introduced. The proper maintenance of the electrical [charge 34] charges 34a, 34b in localized regions of the silicon nitride layer 30 is needed for the proper performance of a two-bit EEPROM device. In particular, the quality of the ONO structure 26 should be such that charge leakage paths are minimized at the interface between the tunnel oxide and top oxide layers 28 and 32, and the silicon nitride layer 30. Additionally, the top oxide layer 32 must be of sufficient density, such that charge trapping sites are minimized within the silicon oxide material.

The amended claims as shown above have been amended as follows:

1. (Amended) A process for fabrication of a semiconductor device including an ONO structure, comprising forming the ONO structure by:

providing a semiconductor substrate having a silicon surface;

forming a first oxide layer on the silicon surface;

depositing a silicon nitride layer on the first oxide layer; and

forming a top oxide layer on the silicon nitride layer,

wherein the first oxide layer is formed by an in-situ steam generation oxidation of the silicon surface and the top oxide layer is formed by an in-situ steam generation oxidation of a surface of the silicon nitride layer.

3. (Amended) The process of [claim 2] claim 1, wherein the semiconductor device is a two-bit EEPROM device in which the first oxide layer is a tunnel oxide layer [, and the tunnel oxide layer is formed by an in-situ steam generation oxidation of the silicon surface].

4. (Amended) The process of [claim 2] claim 1, wherein the semiconductor device is a floating gate EEPROM device in which the first oxide layer is a bottom oxide layer [, and the bottom oxide layer is formed by an in-situ steam generation oxidation of the silicon surface].

5. (Amended) The process of claim 1, wherein the steps of forming [an] a first oxide layer and forming a top oxide layer [, depositing a silicon nitride layer and forming a top oxide layer] are carried out in an RTP [and RTCVD] apparatus.

6. (Amended) The process of claim 1, wherein the steps of forming [an] a first oxide layer, depositing a silicon nitride layer and forming a top oxide layer are carried out in a single-wafer cluster tool.

9. (Amended) The process of claim 1, wherein [the] each step of in-situ steam generation oxidation is carried out at a temperature in the range from about 850°C to about 1150°C.

14. (Amended) A process for fabrication of a semiconductor device, the device including a two-bit EEPROM device including an ONO structure, comprising forming the ONO structure by:

providing a semiconductor substrate having a silicon surface;

forming a tunnel oxide layer overlying the silicon surface by in-situ steam generation oxidation of a portion of the silicon surface;

depositing a silicon nitride layer overlying the tunnel oxide layer; and

forming a top oxide layer overlying the silicon nitride layer by in-situ steam generation oxidation of a portion of the silicon nitride layer.

15. (Amended) The process of claim 14, wherein the steps of forming a tunnel oxide layer [, depositing a silicon nitride layer] and forming a top oxide layer are carried out in an RTP apparatus which is a component of a single-wafer cluster tool.

17. (Amended) The process of [claim 12] claim 14, wherein each step of in-situ steam generation oxidation is carried out at a temperature in the range from about 850°C to about 1150°C and by providing hydrogen gas and oxygen gas to the RTP apparatus.

18. (Amended) A process for fabrication of a semiconductor device, the device including a floating gate FLASH structure comprising an ONO structure, comprising forming the ONO structure by:

providing a semiconductor substrate having a floating gate electrode;

forming a bottom oxide layer overlying the floating gate electrode by in-situ steam generation oxidation of a portion of a surface of the floating gate electrode;

depositing a silicon nitride layer overlying the tunnel oxide layer; and

forming a top oxide layer overlying the silicon nitride layer by in-situ steam generation oxidation of a portion of the silicon nitride layer.

[20.] 19. (Amended) The process of claim 18, wherein the steps of forming a bottom oxide layer, depositing a silicon nitride layer and forming a top oxide layer are carried out in an RTP apparatus which is a component of a single-wafer cluster tool.

[21.]20. (Amended) The process of claim 18, wherein the silicon nitride is deposited by RTCVD.

[22.]21. (Amended) The process of claim 18, wherein each step of in-situ steam generation oxidation is carried out at a temperature in the range from about 850°C to about 1150°C and by providing hydrogen gas and oxygen gas to the RTP apparatus.

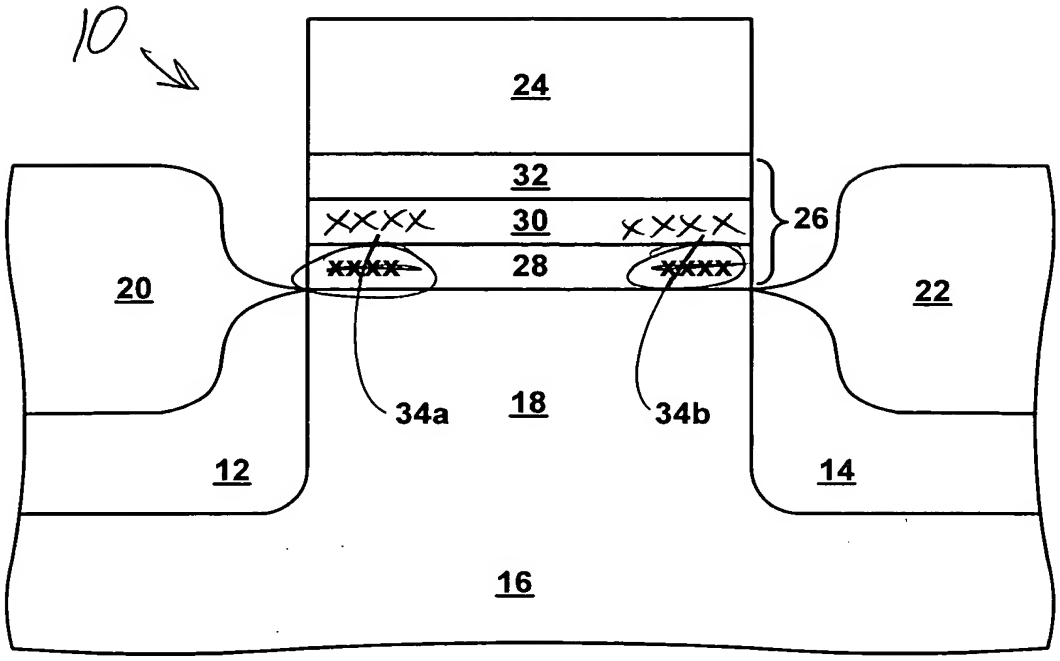

Fig. 1

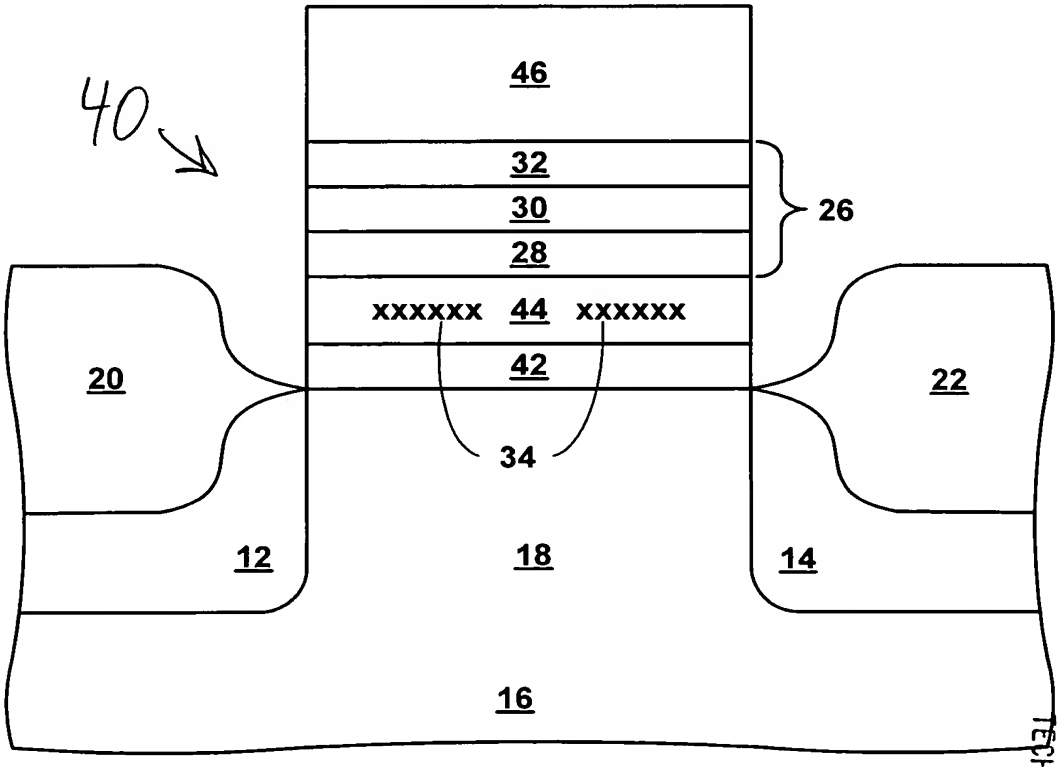

Fig. 2

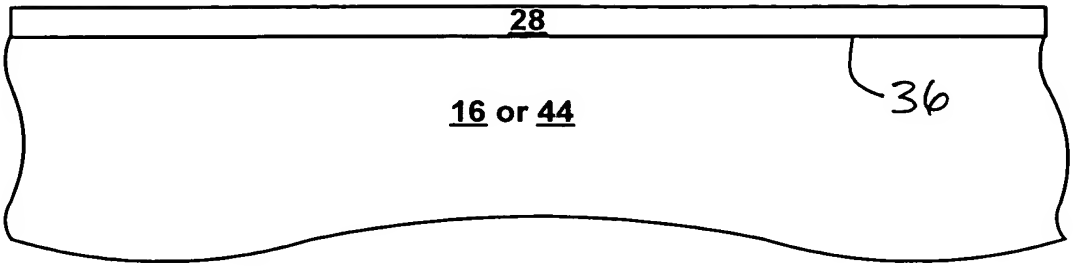

Fig. 3

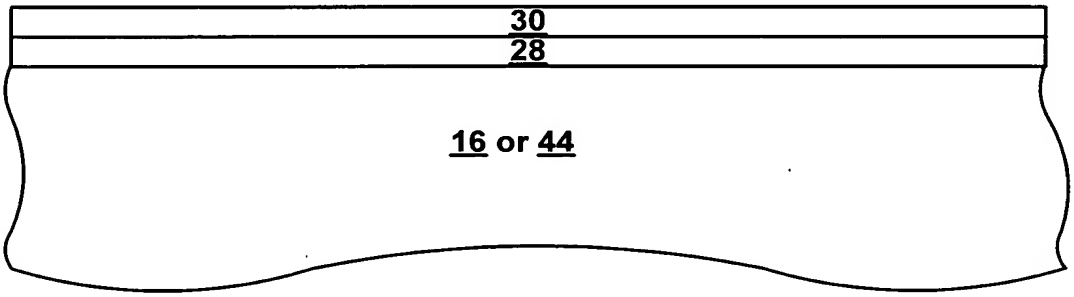

Fig. 4

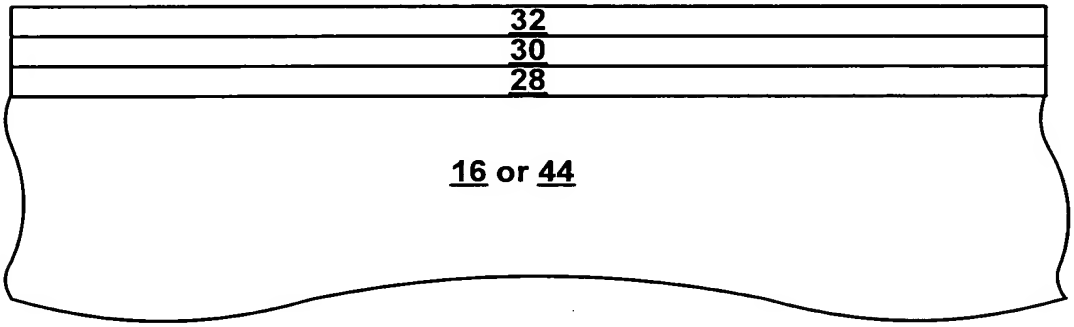

Fig. 5

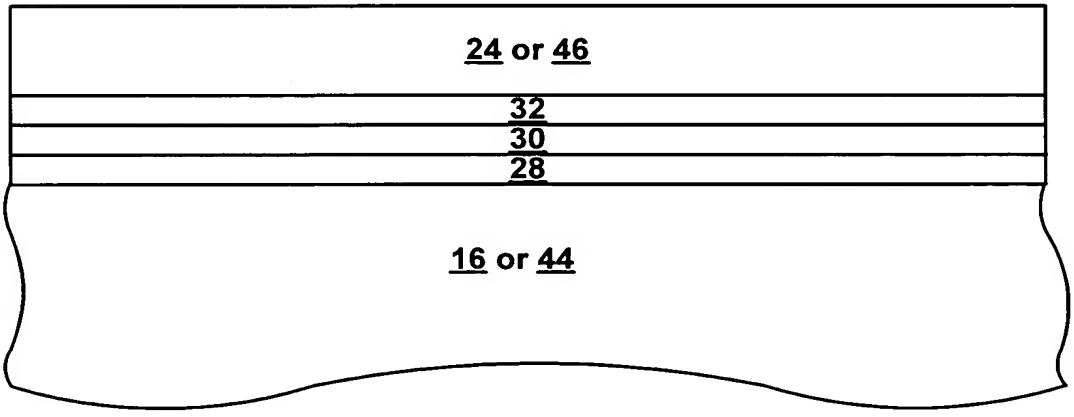

Fig. 6